CLAIMS

What is claimed is:

1. A packaging process for a semiconductor package, comprising the steps of:

1) preparing a substrate having a first surface and a second surface, wherein at least one chip-mounting area is formed on the first surface;

2) disposing a plurality of conductive elements on the chip-mounting area of the substrate, wherein the conductive elements are electrically connected to the substrate and each formed with a flat end;

3) forming a first encapsulant on the chip-mounting area of the substrate for encapsulating the conductive elements, wherein the first encapsulant has a top surface coplanarly formed with the ends of the conductive elements, and the ends of the conductive elements are exposed to the outside of the first encapsulant;

4) mounting at least one semiconductor chip having a plurality of bond pads on top surface of the first encapsulant in a manner that the bond pads face the substrate, wherein the bond pads are electrically connected to the exposed ends of the conductive elements respectively;

5) forming a second encapsulant on the first surface of the substrate for encapsulating the chip; and

6) implanting a plurality of solder balls on the second surface of the substrate, wherein the solder balls are electrically connected to the substrate.

2. The packaging process of claim 1, wherein the conductive elements are conductive bumps.

3. The packaging process of claim 2, wherein the conductive bumps are made of tin, lead

or tin/lead alloy.

4. The packaging process of claim 1, further comprising a step of polishing the first encapsulant and the conductive elements after the step 3) of forming the first encapsulant.

5. The packaging process of claim 1, wherein the chip-mounting area is formed with a plurality of bond pads thereon for being bonded to the conductive elements, and the bond pads are electrically connected to the substrate.

6. The packaging process of claim 1, wherein the chip has a surface with no bond pads formed thereon encapsulated by the second encapsulant.

7. The packaging process of claim 1, wherein the chip has a surface with no bond pads formed thereon exposed to the outside of the second encapsulant for directly contacting the atmosphere.

8. The packaging process of claim 1, further comprising a step of attaching a heat sink to the first surface of the substrate after the step 4) of mounting the chip on the substrate, allowing the heat sink to be encapsulated by the second encapsulant in the step 5) of forming the second encapsulant.